

What is claimed is:

- 1 1. A method for testing a processor including an execution stage comprising:  
2 generating a neutral instruction;  
3 providing said neutral instruction to execution stage of said processor; and  
4 executing said neutral instruction to ascertain an architectural state value for said  
5 processor.
- 1 2. The method of claim 1 wherein said neutral instruction is generated when a plurality of  
2 instructions are generated by a compiler.
- 1 3. The method of claim 1 wherein said neutral instruction is generated by a No-operation  
2 (NOP) pseudo-random generator.
- 1 4. The method of claim 3 wherein the execution of said neutral instruction causes said  
2 processor to access a value stored in a register in said processor.
- 1 5. The method of claim 1 wherein the execution of said neutral instruction causes said  
2 processor to access a value stored in a register in said processor.
- 1 6. The method of claim 1 wherein said neutral instruction is generated by a post-processor  
2 device.

1 7. A system for testing a processor including an execution stage comprising:  
2 comparison logic coupled to the execution stage of said processor, wherein said  
3 execution unit is execute a neutral instruction to ascertain an architectural state value for said  
4 processor.

1 8. The system of claim 7 wherein said neutral instruction is generated by a compiler.

1 9. The system of claim 7 further comprising:  
2 a No-operation (NOP) pseudo-random generator coupled to the execution unit of said  
3 processor to generate said neutral instruction.

1 10. The system of claim 9 wherein the processor includes a register and the execution of said  
2 neutral instruction causes said processor to access a value stored in the register in said processor.

1 11. The system of claim 10 wherein said neutral instruction includes XORing the contents of  
2 said register with itself.

1 12. The system of claim 10 wherein said neutral instruction includes ANDing the contents of  
2 said register with all binary 1 values.

1 13. The system of claim 10 wherein said neutral instruction includes ORing the contents of  
2 said register with all binary 0 values.

1 14. A set of instructions residing in a storage medium, said set of instructions capable of  
2 being executed in an execution stage by a processor for implementing a method to test the  
3 processor, the method comprising:

4 generating a neutral instruction;  
5 providing said neutral instruction to the execution stage of said processor; and  
6 executing said neutral instruction to ascertain an architectural state value for said  
7 processor.

1 15. The set of instructions of claim 14 wherein in said method said neutral instruction is  
2 generated when a plurality of instructions are generated by a compiler.

1 16. The set of instructions of claim 14 wherein in said method said neutral instruction is  
2 generated by a No-operation (NOP) pseudo-random generator.

1 17. The set of instructions of claim 16 wherein in said method the execution of said neutral  
2 instruction causes said processor to access a value stored in a register in said processor.

1 18. The set of instructions of claim 14 wherein in said method the execution of said neutral  
2 instruction causes said processor to access a value stored in a register in said processor.

1 19. The set of instructions of claim 14 wherein in said method said neutral instruction is  
2 generated by a post-processor device.